WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a plurality of word lines each extending in a first direction;

a plurality of bit lines each extending in a second direction crossing said first direction;

a straight active region extending in a direction different from said first and second directions, said active region crossing three or more word lines and three or more bit lines; and

a plurality of memory cells formed in said active regions.

2. The device as claimed in claim 1, wherein each said memory cell includes a data storage capacitor, a first switching element connected to said data storage capacitor, and a second switching element connected to said data storage capacitor.

3. The device as claimed in claim 2, said device further comprising:

a capacitor contact connected to the data storage capacitor and formed on said active region between the adjacent first and second word lines;

a first bit line contact connected to a first one of said bit lines and arranged such that said first word line is sandwiched between said capacitor contact and said first bit line contact; and

a second bit line contact connected to a second one of said

bit lines and arranged such that said second word line is sandwiched between said capacitor contact and said second bit line contact.

4. The device as claimed in claim 1, wherein said active region substantially extends from end to end of a memory cell array area.

5. The device as claimed in claim 1, said device further comprising:

a plurality of bit line contacts each connected to a single bit line, there being four word lines between the adjacent bit line contacts.

6. The device as claimed in claim 2, said device further comprising:

a first row decoder driving a first set of said word lines, said first set coupled to said first switching elements;

a second row decoder driving a second set of said word lines, said second set coupled to said second switching elements, said second row decoder receiving a row address signal;

a first column decoder selecting a first group of said bit lines, said first group coupled to said first switching elements; and

a second column decoder selecting a second group of said bit lines, said second group coupled to said second switching elements, said second column decoder receiving a portion of said row address signal.

7. The device as claimed in claim 6, wherein when said second row decoder drives said second set of said word lines based on one of incrementing and decrementing of said row address signals, said second column decoder alternatively selects the bit lines adjacent to each other among said second group.

8. The device as claimed in claim 2, said device further comprising:

a first row decoder driving a first set of said word lines, said first set coupled to said first switching elements, said first row decoder being activated when data access is performed to a selected memory cell;

a second row decoder driving a second set of said word lines, said second set coupled to said second switching elements, said second decoder receiving a refresh address signal;

a first column decoder selecting a first group of said bit lines, said first group coupled to said first switching elements; and

a sense amplifier circuit sensing a second group of said bit lines, said second group coupled to said second switching element, said sense amplifier circuit being controlled by a sense enable signal and not controlled by an address signal.

9. A semiconductor memory device comprising:

a plurality of word lines;

a plurality of bit lines;

an active region formed on a semiconductor substrate and defined by an element separation region, a boundary between said active region and said element separation region being substantially straight between at least three adjacent word lines; and

a plurality of memory cells formed on a semiconductor substrate.

10. The device as claimed in claim 9, wherein each said memory cell includes a data storage capacitor, a first switching element connected to the data storage capacitor, and a second switching element connected to the data storage capacitor, each of said memory cells connected to a corresponding one of said word lines and a corresponding one of said bit lines.

11. The device as claimed in claim 10, said device further comprising:

a capacitor contact connected to the data storage capacitor and formed on said active region between the adjacent first and second word lines;

a first bit line contact connected to a first one of said bit lines and arranged such that said first word line is sandwiched between said capacitor contact and said first bit line; and

a second bit line contact connected to a second one of said bit lines and arranged such that said second word line is sandwiched between said capacitor contact and said second bit line.

12. The device as claimed in claim 9, wherein said active region substantially extends from end to end of a memory cell array area.

13. The device as claimed in claim 9, said device further comprising:

a plurality of bit line contacts each connected to a single bit line, there being four word lines between the adjacent bit line contacts.

14. The device as claimed in claim 9, said device further comprising:

a first row decoder driving a first set of said word lines, said first set coupled to said first switching elements;

a second row decoder driving a second set of said word lines, said second set coupled to said second switching elements, said second row decoder receiving a row address signal;

a first column decoder selecting a first group of said bit lines, said first group coupled to said first switching elements; and

a second column decoder selecting a second group of said bit lines, said second group coupled to said second switching elements, said second column decoder receiving a portion of said row address signal.

15. The device as claimed in claim 14, wherein

when said second row decoder drives said second set of said word lines based on one of incrementing and decrementing of said

row address signals, said second column decoder alternatively selects the bit lines adjacent to each other among said second group.

16. The device as claimed in claim 9, said device further comprising:

a first row decoder driving a first set of said word lines, said first set coupled to said first switching elements, said first row decoder being activated when data access is performed to a selected memory cell;

a second row decoder driving a second set of said word lines, said second set coupled to said second switching elements, said second decoder receiving a refresh address signal;

a first column decoder selecting a first group of said bit lines, said first group coupled to said first switching elements; and

a sense amplifier circuit sensing a second group of said bit lines, said second group coupled to said second switching element, said sense amplifier circuit being controlled by a sense enable signal and not controlled by an address signal.

17. A semiconductor memory device comprising:

a first row decoder driving at least first and second word lines;

a second row decoder driving at least third and fourth word line;

first, second and third bit lines;

a first memory cell having a first capacitor, a first

switching element coupled between said first capacitor and said first bit line and coupled to said first word line, and a second switching element coupled between said first capacitor and said second bit line and coupled to said third word line; and

a second memory cell having a second capacitor, a first switching element coupled between said second capacitor and said first bit line and coupled to said second word line, and a second switching element coupled between said second capacitor and said third bit line and coupled to said fourth word line.

18. The device as claimed in claim 17, said device further comprising:

a first column decoder selecting at least said first bit line;

a second column decoder selecting at least said second and third bit lines, said second column decoder receiving a portion of a row address signal.

19. The device as claimed in claim 17, said device further comprising:

a first sense amplifier coupled to said first bit line and controlled by a first sense enable signal;

a second sense amplifier coupled to said second bit line and controlled by a second sense enable signal; and

a third sense amplifier coupled to said third bit line and controlled by said second sense enable signal.

20. The device as claimed in claim 19, wherein said second

and third sense amplifiers are not controlled by a row address signal.

21. The device as claimed in claim 17, wherein said first and second memory cells are formed on an active region which are designed in an elongate shape, an edge of said active region does not have a bent portion between said first and second memory cells.

22. The device as claimed in 21, wherein each of said first to fourth word lines extends in a first direction, each of said first to third bit lines extends in a second direction, said active region extends in a third direction different from said first and second directions.